

Abstract - High-K Metal-Gate Designs for Low-Power Applications

Low power has become a design imperative well beyond the traditionally power averse consumer handheld market. Power constraint is the number one cited issue by semiconductor designers regardless of the application space they are addressing. This trend can only be expected to continue in our quest for greener technologies and continuous demand for smaller form factor with longer battery life. Gate dielectrics have not scaled since 90nm largely due to the markets refusal to absorb the unavoidable exponential static power consumption such scaling would cause with traditional transistor devices using Polysilicon Oxynitride (Poly/SiON) gates.

The innovation of High-K metal gate as a replacement for conventional Poly/SiON gate has broken down the scaling barriers providing significant power/performance advantages while allowing geometry shrinks. For the first time we are able to combine gate scaling together with innovations from strain engineering and back end wiring incorporating ultra-low k dielectrics. This session will focus on the advantages these innovations offer in areas ranging from library elements to full product designs. In the first paper we will show Si results of Infineon's digital and analog IP circuits; demonstrating that HKMG can significantly boost large circuit performance beyond that expected with Poly/SiON for 32nm. Additionally, high-yielding SRAM and PLL results give strong indications of HKMG manufacturability. In the second paper Samsung will discuss a concept to accelerate the benefits of HKMG and how to optimize designs through Design Methodology. Finally, they will show the plan to adopt this innovative technology to the next stage mobile product development.

Organizer: Ana Hunter, Vice President, Foundry, Samsung Semiconductor, Inc.

Digital and Analog Circuit Demonstration of HKMG for 32nm

Speaker:

Dr. Richard Lindsay, 32nm Technology Project Mgr, Infineon Technologies, Inc.

Contributors:

M. Eller, J-P Han, M. Ostermayr, C. Pacha, K. vonArmin, K. Schroefer, J. Einfeld, Infineon Technologies

Product Innovation Made Possible with 32-nm HKMG

Speaker:

Dr. K.M. Choi, Vice President, Design Technology, System LSI Division, Samsung Electronics

Abstract - HKMG fundamentals and its application to 32nm Technology

As the physical limits of CMOS technology are approached, alternative innovative techniques are required in order to achieve the continued scaling of silicon solutions consistent with the power and performance expectations of converged applications in volume markets. As we chase the immutable dictate of Moore's Law, new techniques that, not too many years ago, were considered outside the realm of achievability are now accessible in a foundry relationship. The Joint Development Alliance (JDA) of Chartered, Freescale, IBM, Infineon, Samsung, STM and Toshiba has introduced in the 32 nm node, High-K, Metal Gate as the optimized approach in support of the new generation of product solutions. This technology is being deployed through the Common Platform manufacturing and enablement alliance of Chartered, IBM, and Samsung. The speakers in this session are preeminent Joint Development Alliance technologists responsible for creation and delivery of the 32nm node. The session will focus on providing information on the unique aspects of HKMG process and device technology. An emphasis will be placed on providing comparisons to previous nodes and the compelling differentiation with Poly SION.

Organizer: Dr. Walter Lange, Vice President, Platform Alliances, Chartered

HKMG fundamentals and its application to 32nm Technology

Speaker:

Dr. An Steegen , 32nm Program Director - IBM

32 nm Device Performance Capabilities and Specifications

Speaker:

Dr. Ron Sampson, Director & Project Leader, IBM Alliances, STMicroelectronics

Abstract - Experiences with 32nm High-K Metal Gate Design

Significant challenges have always been present for leading edge chip design, especially as process technologies shrink. Lithography, design complexity, power consumption, and variability issues have only become more challenging and have been projected to become even more evident at 32nm. In some technologies it has been projected that design is becoming an over constrained problem, making it challenging to achieve optimal performance. In the marketplace where battery life and performance are both absolute requirements it is now essential to embrace new models that drive closer collaboration and innovation. This talk highlights the long history of partnership with the Common Platform at 90/65/45nm and more recently tighter collaboration at 32nm. Specifically, the key features of a 32nm test chip produced by ARM for the September shuttle will be described. The chip contains multiple CPUs synthesized from a standard cell library along with sample memories using 3 different bit cells and some innovative measurement structures to optimize the electrical properties of the new high K metal gate process. ARM and the Common Platform cooperated extensively in order to produce this chip on topics ranging from design rules, device models, and CPU performance. Details on the chip and on the cooperative development partnership that is creating world class solutions are provided.

Organizer: Mark Ireland, Vice President, Semiconductor Platforms, IBM

Speaker: Dr. Robert C. Aitken, R&D Fellow, ARM

Abstract - Energy Aware Multi-Processing With ARM Cortex™-A9 MPCore™

Multiprocessing CPU architectures can now be employed to address the increasing demand for mobile performance while at the same time helping to manage power consumption and the ARM Cortex-A9 MPCore processor has been developed for that very purpose. Implementing high performance CPUs while at the same time minimizing power consumption is becoming ever more challenging as we move rapidly to very small geometries of 45nm and 32nm. In order to meet this challenge, the concurrent optimization of power and performance during the implementation process is critical as is the need for identifying and employing the most efficient low power methodology.

This talk will discuss in technical detail a number of low power strategies that were employed during the implementation of a 45nm dual-core ARM Cortex-A9 MPCore processor to yield ultra low power while providing the performance levels required. The talk will highlight specific features of the Cortex-A9 MPCore architecture that enable a low power implementation and discuss the power vs. performance challenges when targeting a leading process from Common Platform.

Details on how these challenges are addressed through an optimal implementation solution with seamless integration of advanced low power physical IP from ARM with the Eclipse Low Power Solution from Synopsys will also be discussed.

Speaker:

Alan Gibbons, Principal Engineer, Synopsys

Contributors:

David Flynn, Fellow, ARM Ltd.

John Biggs, Co-Founder & Methodology Consultant, ARM Ltd.

Abstract - Advanced Technology for Density and Performance Scaling

The recent introduction of a new line of application processors is leveraging an innovation in material science, called high-K, metal gate, to provide performance in low-power, low-leakage SOC application processors for un-tethered mobile internet application devices. The IBM-led Joint Development Alliance (JDA) collaboration, which also includes Chartered, IBM, Infineon, Samsung, ST Microelectronics and Toshiba, is not only matching this innovation but also providing an open, collaborative model with a robust design ecosystem, including ARM, which is keeping the fabless industry competitive with the IDM proprietary model. To remain competitive, however, requires a never-ending treadmill of technology introduction and new innovation. The IBM-led collaborative innovation pipeline is a distinctive strategic advantage set up to feed the JDA and Common Platform. In this session two leading edge technologists describe key aspects of the technology innovation roadmap that enable the next generation pipeline of technology and solutions that will keep the fabless industry competitive.

Organizer: Kevin Meyer, Vice President, Industry Marketing and Platform Alliances, Chartered

Computational Lithography and its application and integration into CMOS Technology

Speaker:

Dr. Dario Gil, Senior Manager, Computational Lithography, T.J. Watson Research

Co-Author:

Tim Farrell, Distinguished Engineer, Computational Technology, IBM

Nanomaterials Innovation in Interconnect Technology

Speaker:

Dr. Jim Ryan, Founding Dean of the Joint School of Nanoscience and Nanoengineering (JSNN) of North Carolina A&T State University and the University of North Carolina at Greensboro

Contributor:

Dr. Ji Ung Lee, Empire Innovation Professor, University at Albany

Abstract - Design Challenges & Methodology Solutions Spanning to 32nm

This technical session is designed to assist designers in navigating the critical choices in developing a state-of-the-art low-power, low-leakage design methodology for mobile applications targeted for process technologies spanning from 65nm to 32nm. As the hype surrounding DFM subsides, the real capabilities required to address manufacturability are being integrated into existing design flows from the major EDA suppliers. However, as has been anticipated, this becomes yet another variable in the design trade-off equation. Designers still need to be focused on achieving timing closure with a signal-integrity clean design while remaining within ever more demanding power and leakage budgets. At 32nm, advanced understanding of manufacturability is now mandatory – not a post design expectation that the foundry will make it yield. This team of experienced EDA technologists, augmented by a customer designing at the leading edge, will detail what they deem to be the greatest technical challenges with a current 45/40nm perspective looking out towards 32nm implementations, and what has been done to address them.

Organizer: Walter Ng, Vice President, Design Enablement Alliances, Chartered

Speakers:

Juan C. Rey, Sr. Engineering Director, Mentor Graphics

Richard Brashears, Corporate Vice President, Manufacturing Modeling and Implementation Technology, Cadence Design Systems

Dr. Tong Gao, Scientist, Synopsys